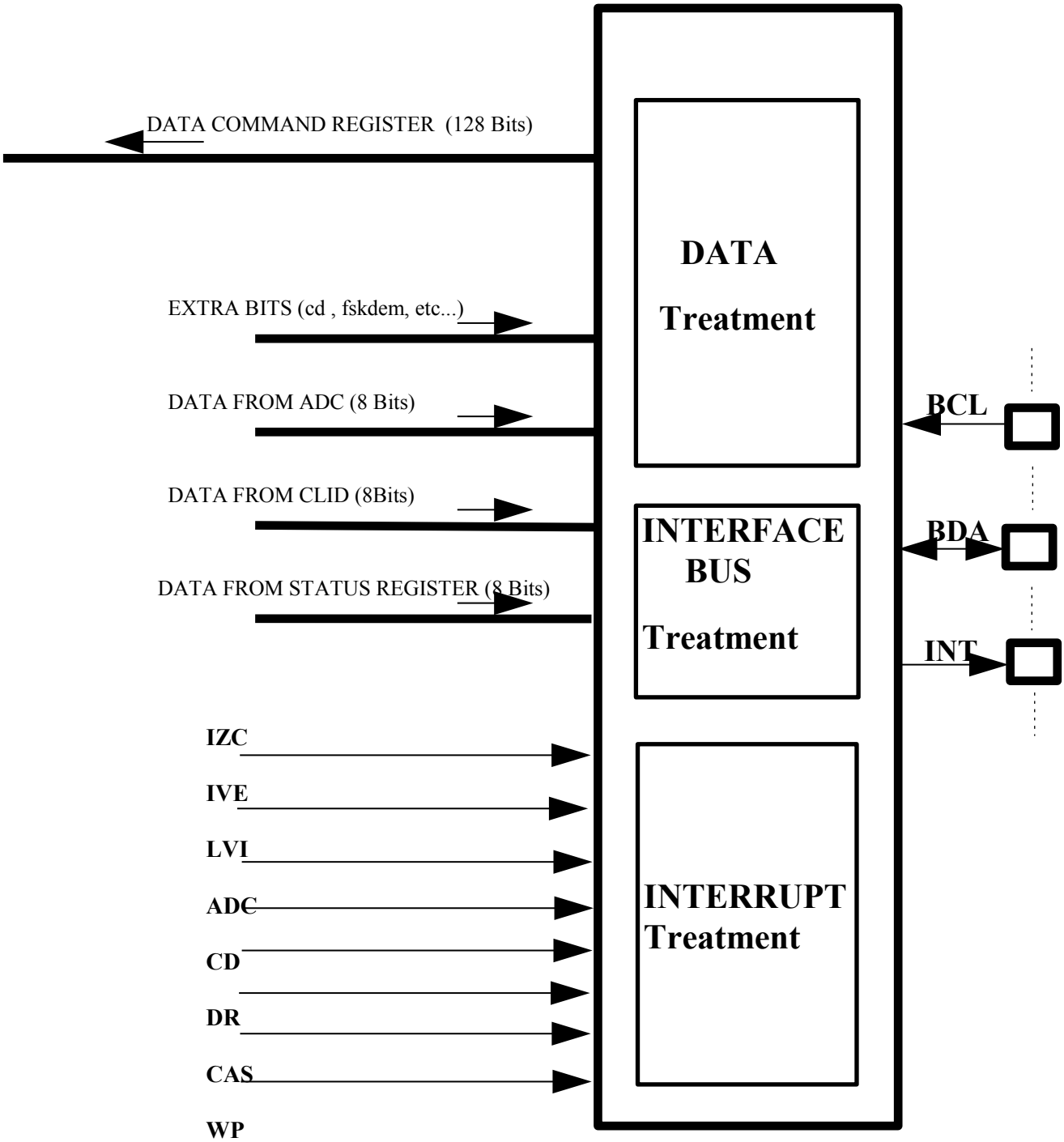
SYNCHRONOUS SERIAL BUS (SSB) OVERVIEW



SYNCHRONOUS SERIAL BUS (SSB)

The SSB BUS is a bi-directional and synchronous serial bus with:

- A « DATA » line: BDA
- A « CLOCK » line: BCL
- An « INTERRUPT » line: INT

The SSB bus can share the 2 lines SDA and SCL of the I2C bus. It is not a I2C compatible bus but a tolerant I2C bus :
when the I2C bus is sleeping the SSB bus can work and much faster !..

This speed feature is particularly useful when extracting CLID data, and extremely useful when watching the events on the line, thanks to a new added feature the **Fast Read Mode.**

The **Fast Read Mode** allow the Microprocessor to access important information very quickly without specifying a register address.
In OCTEL3 two information are important: IZC and IVE.

When the Microprocessor initiates a Fast Read Mode these information are on the bus. Such a speed access is not possible with an **I2C bus.**

The «DATA » line carry the address bits, the data bits, the R/W bit and the Strobe.
The address bits are 4 in normal mode. There is not address bit in Fast Read mode.
The DATA format is 8 bits in Write and Read Normal mode, 2 bits in Fast Read mode.
The Strobe is created by a falling and a rising edge while the CLOCK line is continuously high.
The «DATA » line is bi-directional that mean: in Write mode the DATA are send from the Microprocessor to the OCTEL3 and in Read mode from the OCTEL3 to the Microprocessor.
The «CLOCK » line is unidirectional. The Data on the «DATA » line must be stable during the High period of the Clock signal. The High or Low state of the Data line can only change when the Clock signal on the «CLOCK » line is Low. The only changes of Data during a High state of Clock are for the STROBE Signal.
The Strobe is created by a falling and a rising edge while the CLOCK line is continuously high.
The «INTERRUPT » line is an open-drain type, because it can be shared with other peripherals.

TRANSFERRING DATA:

In Write mode, data are loaded with the strobe signal (8bits).
There are 16 registers of 8 bits (total: 128 bits)
In normal Read mode, addresses are loaded with the strobe signal. After that, Data is send to the Microprocessor (8bits).
There are 4 readable registers:
Add 0: The STATUS register.
Add 1: The DATA CLID register.
Add2: The DATA ADC register.
Add3: The EXTRA bits register with the Carrier Detect signal, the demodulated data and b2 to b7, R12 register bits. (available on third run pieces)
In Fast Read mode after the strobe, Data is sent to the Microprocessor (2bits).
In OCTEL3 the 2 bits sent are IZC and IVE.

SSB INTERRUPT TREATMENT

There are 8 possibilities to interrupt the Microprocessor:

- IZC : Zero Crossing Current.
- IVE : Line Voltage Information.
- LVI : Low Voltage Information.
- ADC: End of ADC treatment.
- CD : CLASS Carrier Detect Signal.
- DR : CLASS Data Ready Signal.
- CAS: CLASS Call Alert Signal.
- WP : CLASS Wetting pulse.

The interrupt can be enabled or disabled with a command bit (MSK_IT). Enabled when R11B7=1.
The interrupt state is a low level outside the OCTEL3 on the INT pin.
This pin is an open-drain type, because it can be shared with other peripherals.
All information about the interrupt sources is on the STATUS REGISTER, the Microprocessor can read it anytime.
The DR and WP bits are cleared after reading the STATUS REGISTER and the INT pin goes at high level.

IT N°	NAME		Rising or Falling active edge	STATUS REGISTER Bit N°
1	IZC	Zero crossing Ringing information	both	7
2	IVE	Line voltage information	both	6
3	LVI	Low Voltage Information	both	5
4	ADC	ADC Treatment	Rising (50µS after SOC. signal)	4
5	DR	CLID Data Ready Signal	Rising Each 8.33 ms	3
6	CD	CLID Carrier Detect Signal	both	2
7	CAS	CLASS Alert Signal	both	1
8	WP	CLASS Wetting Pulse	Falling. 15 ms after the end of CAS	0