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(72) NIHOUARN, Gilbert, FR
(71) MATRA NORTEL COMMUNICATIONS, FR

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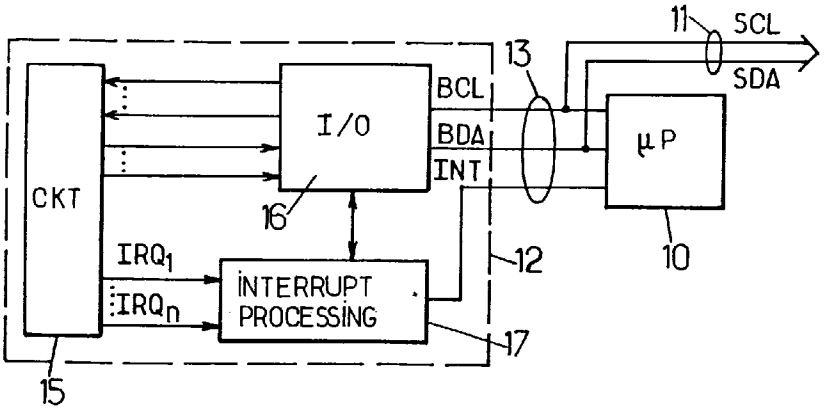
(54) **PROCEDE DE TRANSFERT SERIE DE DONNEES ET INTERFACE DE BUS SERIE SYNCHRONE METTANT EN OEUVRE CE PROCEDE**

(54) **SERIAL DATA TRANSFER PROCESS, AND SYNCHRONOUS SERIAL BUS INTERFACE IMPLEMENTING SUCH PROCESS**



(57) The synchronous serial bus (13) between a main processing unit (10) and a peripheral unit (12) includes a data line (BDA) and a clock line (BCL). Strobe pulses presented by the main processing unit (10) on the data line while it holds the clock line at a given logic level characterise transfer cycles on the bus (13). The main processing unit (10) can thus run write or read cycles in registers of an interface (16) of the peripheral unit (12). A direct transfer mode, wherein the strobe pulse is transmitted at the beginning of the cycle without specifying an address, is provided to enable the main processing unit (10) to have a fast access to certain locations previously specified. The data and clock lines (BDA,BCL) of the bus (13) may be shared with those of another synchronous bus (11).